REMARKS

As a preliminary matter, Applicant respectfully requests entry of this after-final amendment because the proposed amendment to Claim 1 does not raise new issues requiring further search or consideration. More specifically, the proposed amendment to Claim 1 merely incorporates the subject matter of associated dependent Claim 7 into Claim 1. Since the subject matter of now-cancelled Claim 7 was previously considered when examining this claim, no new issues requiring further search or consideration are raised by combining Claim 7 with associated independent Claim 1. Accordingly, entry and consideration of the after-final amendment is respectfully requested.

Claims 1-14 and 17-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanbe et al. (U.S. Patent No. 6,151,016) in view of Yasui et al. (U.S. Patent No. 5,248,963). Applicant respectfully traverses this rejection as it applies to the newly-amended claims.

Regarding newly-amended Claim 1, Applicant asserts that Kanbe et al. and Yasui et al., alone or in combination, fail to disclose or suggest the features of the recited claim. More specifically, the Kanbe et al. reference fails to disclose a liquid crystal display device including at least the following feature: "wherein, after the input power supply is cut off, a voltage based on said second power supply is outputted to all gate signal lines of the display part" as now recited in Claim 1.

In the present invention of Claim 1, the voltage input Vin is supplied to the all-output-on terminal Vxon. When this signal becomes low, the gate-driving circuit 4

asynchronously outputs a voltage to all outputs VOUT1, VOUT2, ..., VOUTn. This output, which is supplied to the gate-driving circuit 4 through the gate-on power supply terminal Vgon, is provided irrespective of other input signals. (See Applicant's Specification, page 9, lns. 1-7)

In contrast, the Kanbe et al. reference merely discloses a gate driving section 3 that drives gates sequentially. That is, the gate driving section 3 drives m gate lines 25_1-25_m on the liquid crystal display panel 1 so that the TFTs 23 on the first through m^{th} gate lines are sequentially turned ON. Upon input of a power source OFF signal, the auxiliary power source 10 provides power for driving the liquid crystal display 1. At that time, the driving signal generating circuit 8 generates a signal to light up the display for at least the time required for a vertical scan of the LCD panel 1 (see Kanbe et al., col. 8, lns. 38-42). The gate lines 25_1-25_m are turned on sequentially by the signal (see Kanbe et al., col. 8, lns. 58-60).

Moreover, the Yasui et al. reference fails to remedy the deficiencies of Kanbe et al. More specifically, the Yasui et al. reference also teaches sequentially activating all the TFTs 13 of the liquid crystal display panel 10. An output clear signal CL is applied for time T, so that all TFTs 13 are turned on, and each pixel 12 is set to ground (see Yasui et al., col. 5, lns. 51-60). Accordingly, Applicant traverses the § 103(a) rejection as it applies to amended Claim 1 because Kanbe et al. and Yasui et al., whether taken alone or in combination, fail to disclose or suggest a voltage based on said second power supply being outputted to all gate signal lines of the display part, as recited in Claim 1.

Regarding independent Claims 8 and 17, Applicant asserts that Kanbe et al. and Yasui et al. fail to disclose or suggest the features of these claims. Specifically, neither Kanbe et al. nor Yasui et al. discloses or suggests a display device that includes *inter alia*, a power supply changeover circuit configured to selectively output as an internal power supply, one of a first power supply and a second power supply.

In the embodiment of the present invention of Claims 8 and 17 shown in Fig. 1, a power supply changeover circuit 3 is provided with inputs of a first power supply (luminance inclination circuit 1) and a second power supply (power holding circuit 2). The power supply changeover circuit 3 selects a signal from either the luminance inclination circuit 1 or the power holding circuit 2 based on the signal Vin, and outputs the selected signal to the gate driving circuit 4 via the gate-on power supply terminal Vgon.

In contrast, the Kanbe et al. reference discloses a power source control circuit 56 that merely controls a relay switch 60. When the power source control circuit 56 applies a high voltage to the relay switch 60, the relay switch allows the power source control circuit to receive power from the main power source. When an OFF signal is received, the power source control circuit 56 applies a low voltage to the relay switch 60, the relay switch becomes non-conductive, and power supply from the main power source is stopped (see Kanbe et al. col. 17, lns. 26-29). Therefore, while the Kanbe et al. reference discloses a means to start and stop the power supply from a main power source, it does not disclose a method of selectively outputting power supply from either a first power source or a second power source.

Again, the Yasui et al. reference fails to alleviate the deficiencies of Kanbe et al. The Examiner asserts that the voltage drop detector 24 corresponds to the power supply changeover circuit of the present invention. However, as can be seen in Fig. 5 of Yasui et al., the voltage drop detector outputs has only a single input V_I and a single output V_B. Moreover, the power circuit 23 and power holding circuit 22, which the Examiner identifies as corresponding to the first power supply circuit (luminance inclination circuit) and the second power supply circuit (power holding circuit) of the present invention, are not provided as inputs to the voltage drop detector 24, nor are they generated within the voltage drop detector. Thus, the voltage drop detector 24 cannot provide signals from either the power circuit 23 or the power holding circuit 22 as outputs.

Therefore, Applicant traverses this rejection as it applies to independent claims 8 and 17 because Kanbe et al. and Yasui et al. whether taken alone or in combination, fail to disclose or suggest a power supply changeover circuit configured to selectively output a first power supply or a second power supply.

Claims 15-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanbe et al. in view of Yasui et al., and in further view of Lee (U.S. Patent No. 7,023,511). Claims 15-16 depend from independent Claim 1, and therefore include all the features of Claim 1, plus additional features. Accordingly, Applicant respectfully requests that the rejection of dependent Claims 15 and 16 be withdrawn in light of the above remarks directed to Claim 1, and because Lee does not remedy the deficiencies identified with respect to the rejection of Claim 1.

Claims 19-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanbe et al. in view of Yasui et al., and in further view of Tsuchi et al. (U.S. Patent No. 6,909,414). Claims 19, 22, and 25 depend from Claim 1, either directly or indirectly. Similarly, Claims 20, 23, and 26 ultimately depend from Claim 8, and Claims 21, 24, and 27 ultimately depend from Claim 17. Because these claims incorporate the limitations of their respective independent claims, and because the Tsuchi et al. reference fails to overcome the identified deficiencies of the rejections of independent Claims 1, 8, and 17, withdrawal of this rejection is respectfully requested.

For all of the above reasons, Applicant submits that this application is in condition for allowance, which is respectfully requested. Should the Examiner be of the opinion that a telephone conference would aid in the prosecution of the application, or that outstanding issues exist, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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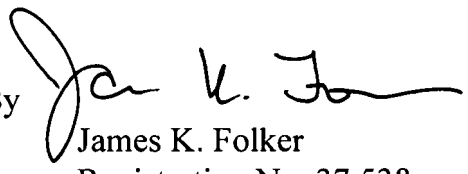
By 

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